

IN THE CLAIMS

- 1 (Previously Presented). An integrated memory system, comprising:
a non-volatile solid-state memory; and
an automatic storage error corrector including functionally independent devices,
each device to correct a different predetermined storage error of data stored in the memory, at least one of said devices being external to the memory.
- 2 (Previously Presented). A system according to claim 1, wherein said memory is connected to a controller by means of an interface bus and said devices are incorporated both in the memory and in the controller.
- 3 (Previously Presented). A system according to claim 1, including coding circuits to correct two errors, a logic to calculate a syndrome, a single error correcting circuit, and a logic to detect more than one error.
- 4 (Previously Presented). A system according to claim 3, further including a logic to supply the controller with a one-or-no-error-corrected data, the uncorrected error, and the calculated syndrome.
- 5 (Previously Presented). A system according to claim 2, including a circuit to generate a signal to request the external correction of an error by said controller.
- 6 (Previously Presented). A system according to claim 3, wherein said coding circuits are located immediately downstream of the input terminal of said memory to perform a vector product proportional to the number of parity bits and obtained through the synthesis of a corresponding logic function.
- 7 (Previously Presented). A system according to claim 6, wherein said logic to calculate the syndrome to use a parity calculation circuit of the coding circuits.

8 (Previously Presented). A system according to claim 3, wherein said single error correcting circuit for an error comprises a block to decode a single error effective to recognize each of the several syndromes associated to a single error to activate, through a corresponding vector, the correction of the corresponding bit.

9 (Previously Presented). A system, comprising:

a first circuit operable to store data in a non-volatile solid-state memory, the data having associated therewith at least one storage error of a plurality of storage-error types, the first circuit operable to correct a first-type error of the plurality of storage-error types; and

a second circuit coupled to the first circuit, the second circuit operable to correct a second-type error of the plurality of storage-error types.

10 (Previously Presented). The system of claim 9 wherein the second circuit to generate a signal requesting correction of a third-type error of the plurality of storage-error types.

11 (Previously Presented). The system of claim 9 wherein the first circuit further to determine at least one syndrome associated with the at least one storage error.

12 (Previously Presented). The system of claim 9 wherein the first circuit further to detect the second-type error.

13 (Previously Presented). The system of claim 9 wherein the second circuit to correct the second-type error in response to a signal generated by the first circuit.

14 (Original). The system of claim 9 wherein the first circuit comprises a non-volatile memory.

15 (Original). The system of claim 9 wherein:

the first circuit is disposed on a first integrated circuit; and

the second circuit is disposed on a second integrated circuit.

16 (Original). The system of claim 9 wherein the first and second circuits are disposed on an integrated circuit.

17 (Previously Presented). A memory device, comprising:
a non-volatile solid-state storage portion to store data having associated therewith at least one storage error of a plurality of storage-error types;
a first circuit to correct a first-type error of the plurality of storage-error types; and
a second circuit to generate a signal indicating detection of a second-type error of the plurality of storage-error types.

18 (Previously Presented). The device of claim 17, further comprising a third circuit to determine at least one syndrome associated with the at least one storage error.

19 (Previously Presented). A method, comprising:
storing, in a non-volatile solid-state memory location of a device, data having associated therewith at least one storage error of a plurality of storage-error types; and
correcting, at the memory location, a first-type error of the plurality of storage-error types.

20 (Original). The method of claim 19, further comprising generating, at the memory location, an interrupt-request signal indicating detection of a second-type error of the plurality of storage-error types.

21 (Previously Presented). An electronic system, comprising:
a first integrated circuit having a non-volatile solid-state memory to store data having associated therewith at least one storage error of a plurality of storage-error types, the memory to correct a first-type error of the plurality of storage-error types; and
a second integrated circuit coupled to the first circuit, the second integrated circuit having processor to correct a second-type error of the plurality of storage-error types.